REMARKS

Claims 1-12 are pending in the application.

Claims 1, 5 and 12 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. It is believed that this Amendment is fully responsive to the Office Action dated **February 13, 2003**.

Objections to the Claims

Claims 1, 5, 12 and 13 are objected to because of various informalities. These claims have been amended, as needed, to overcome this objection. Indeed, the claimed invention does not form any silicon nitride film.

Reconsideration and withdrawal of this objection are respectfully requested.

Claim Rejections under 35 USC §103

Claims 1, 3 and 12 are rejected under 35 USC §103(a) as being unpatentable over Arita et al. (U.S. Patent No. 6,046,490) in view of Zhang (U.S. Patent No. 5,990,491).

Claims 2 and 4 are rejected under 35 USC §103(a) as being unpatentable over Arita et al. (U.S. Patent No. 6,046,490) and Zhang (U.S. Patent No. 5,990,491) as applied to claim 1 above, and further in view of Singh et al. (U.S. Patent No. 5,847,464).

Claims 5 and 9-11 are rejected under 35 USC §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. (U.S. Patent No. 6,046,490) and Zhang (U.S. Patent No. 5,990,491).

Claims 6-8 are rejected under 35 USC §103(a) as being unpatentable over Mochizuki et al. (U.S. Patent No. 5,990,507) in view of Arita et al. (U.S. Patent No. 6,046,490) and Zhang (U.S. Patent No. 5,990,491), as applied to claim 5 above, and further in view of Singh et al. (U.S. Patent No. 5,847,464).

The present invention contains nitrogen residing all over the surface of the silicon oxide film. These features prevent moisture from entering into the capacitor through the silicon oxide without a silicon nitride film.

In contradistinction, the asserted prior art Arita or Zhang needs to form a silicon nitride film on a silicon oxide film to prevent moisture from entering into the silicon oxide film.

Therefore, the claimed invention provides a technical breakthrough overcoming the technical limitations of Arita and Zhang.

Independent claims 1, 5 and 12 respectively provide a feature that the contact is positioned above the silicon oxide film including nitrogen, the contact is positioned above the fourth insulating film including nitrogen, and the contact is positioned above the second insulating film including nitrogen. The purpose of reciting a "contact" into these claims is to make sure that there is a clear understanding that the silicon oxide film including nitrogen are position beneath the "contact."

In contradistinction, in Mochizuki, there is no disclosure or teaching of a silicon oxide film including nitrogen beneath a contact.

The above-mentioned differentiations between the asserted prior art references and the claimed invention clearly support the fact the claimed invention is not rendered obvious by the asserted prior art. In fact, even if the asserted prior art references are combined, exactly as suggested

in the outstanding Office action, the claimed invention would not result.

Independent claims 1, 5 and 12, as newly amended, are patentably distinguished over the asserted prior art. All claims dependent thereon, by virtue of inherency, are also patentably distinguished over the asserted prior art.

Reconsideration and withdrawal of this rejection are respectfully requested.

Prior Art Indicated To Be Pertinent To The Disclosure

The Office has provided a list of prior art indicated to be pertinent to the Applicant's invention. Consistent with the understanding as stipulated in MPEP 706.02 that only the best prior art should be applied, this list of prior art not having been applied by the Office, it is the Applicant's understanding that the Office must have considered the listed prior art to be no more pertinent than the applied prior art of record.

Conclusion

In view of the aforementioned amendments and accompanying remarks, claims 1, 5 and 12, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/594,091

IN THE CLAIMS:

Please amend claims 1, 5 and 12 as follows:

1. (Thrice Amended) A semiconductor device, comprising:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween; and

a silicon oxide film residing on top of the capacitor to form a planarized surface;

wherein nitrogen resides over the planarized surface of the silicon oxide film; and

wherein the contact is positioned above the silicon [nitride] oxide film including nitrogen.

5. (Thrice Amended) A semiconductor device, comprising:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film residing on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric made of

one of ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film formed on the capacitor;

a local interconnection formed on the second insulating film to electrically connecting the upper electrode of the capacitor with the first impurity region;

a third insulating film formed on the local interconnection and the second insulating film;

a first wiring formed on the third insulating film and electrically connected to the second impurity region via a hole which is formed on the first insulating film, the second insulating film, and the third insulating film;

a fourth insulating film on top of the first wiring to serve an upper planarized surface,

wherein nitrogen resides on top of the upper planarized surface of the fourth insulating film;

wherein the contact is positioned above the [silicon nitride] <u>fourth insulating</u> film including nitrogen; and

a second wiring formed on the fourth insulating film.

12. (Thrice Amended) A semiconductor device, comprising:

a contact;

a transistor having a first impurity region and a second impurity region formed on a semiconductor substrate, and a gate electrode formed on the semiconductor substrate;

a first insulating film on top of the transistor;

a capacitor formed on the first insulating film, the capacitor having a dielectric film made of one of a ferroelectric material and a high-dielectric material, and an upper electrode and a lower electrode positioned to put the dielectric film therebetween;

a second insulating film on top of the capacitor to serve as an upper planarized surface;

wherein nitrogen resides on top of the upper planarized surface of the second insulating film; and

wherein the contact is positioned above the [silicon nitride] second insulating film including nitrogen.